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# NEW HIGH PERFORMANCE 8T SRAM CELL USING FINFET TECHNOLOGY

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**Abstract**

In the design of memory, the estimation of dynamic power, dynamic current, leakage current and power of leakage are very essential, especially for low power applications. In this paper, we propose a FinFET base 8T Static Random Access Memory (SRAM) cell. FinFETs also promise to improve the difficult performance report power of compromise. FinFET can be used to reduce the leakage current and power of leakage. The purpose of this paper is to reduce the leakage current, power and improve the power of FinFET based 8T SRAM cell. The present paper represents the simulation of 8T and the analysis of SRAM different parameters such as power dissipation, leakage current and power of leakage. By this paper the leakage current improve 4.35 nA to 2.83 nA and leakage power 16.60 nW to 11.35 nW. The WSNM is 530.30 and RSNM is 516.70Mv. In this paper we use Empyrean Aether tools at 22 nm technology.

***Keywords:***
SRAM Cell;
FinFET;
Leakage Current;
Leakage Power;
WSNM and RSNM.

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## 1. Introduction

Static Random Access Memories (SRAMs) have become an important part of modern electronics. SRAMs are faster compared to Dynamic Random Access Memories (DRAMs) and do not require clocking or frequent refreshing to store the data. The data stored in SRAMs remains stable until power is applied to it. Due to these features of SRAMs, they are mainly used in the cache memory of microprocessors.

Large area of modern-day chips are occupied by SRAMs. On – die cache memory is ever increasing to achieve higher performance benefits in modern microprocessors, portable, mobile and handheld applications in each new technology generation [1]. Thus, the CMOS IC technology has been continuously scaled down to enter the nanometer regime. As the technology scaling enters the nanometer regime, significant challenges such as reliability issues, process variations and Short Channel Effects (SCEs) are faced [2]. Scaling reduces the gate's control on the channel which degrades the performance of the device. SCEs result in undesirable sub-threshold leakage currents. In severe cases, SCEs may also affect the other devices in the chip. Using thinner gate oxide in MOS transistor reduces SCEs at the cost of more power and less reliability [3]. New devices are suggested to overcome SCEs instead [4]-[5]. FinFETs are one of the best devices among these towards deep nanometer technology nodes.

FinFET devices provide superior control on the channel subduing SCEs, lower leakage current and higher ON current compared to CMOS counterpart [6]. They show greater scalability, insensitivity to random variations and better choice of nanometre technology [7]. Hence, robust and energy-efficient SRAM cell designs can be achieved by using FinFET technology.

For conventional 8T SRAM cell there is an additional requirement of a bitline to improve the stability performance of the cell adhering to area overhead. The proposed FinFET 8T SRAM cell improves both leakage current and leakage power relative to conventional 6T and 8T SRAM cells while maintaining less cell delay and low power using FinFET technology.

## 2. Conventional 8T SRAM Cell

Conventional 8 Transistor SRAM cell is shown in Fig 1 [10]. In this, conventional 6 Transistor SRAM cell acts as the core. Two additional n-type transistors with an additional bitline (RB) and control signal (RWL) are used to isolate the cell core from the output. Write operation is performed via access transistors (PG2-PG1) and bitlines WBL and WBLB. The read operation is performed via RG1 and RG2. The data stored in the cell appears on the read bitline RB. PG1 and PG2 are made stronger than PU1 and PU2 for successful write operation.

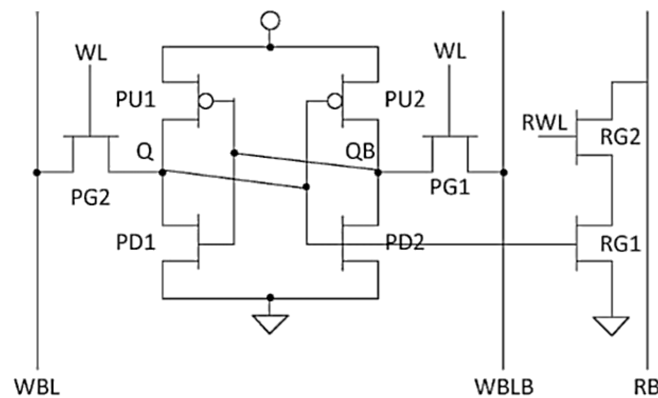


**Fig.1 Conventional 8T SRAM Cell**

## 3. FinFET Technology

The FinFET transistor is a vertical double-gate device and is regarded as a promising alternative for sub-22 nm bulk devices [8]. A unique property of the FinFET is the electrical coupling between the front and back gates. The implication of this coupling is that the threshold voltage of the front gate (Vthf) is not only established by the process, but also it can be controlled by the Back Gate Voltage (VGb). This is similar to the body effect in a bulk transistor [9].

The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon “fin”, which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device.

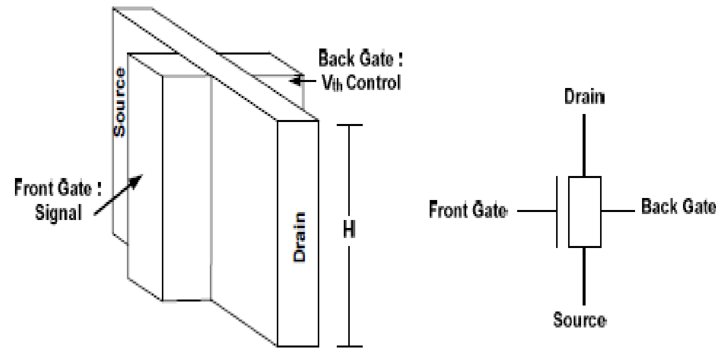


**Fig. 2 FinFET Structure and Symbol**

Fig. 2 shows the structure of a multi-fin double gate FinFET device. Current flow is parallel to the wafer plane. The thickness t is of the single fin is equal to the silicon channel thickness. Each fin contributes to the width of the device, and H is the height of each fin.

**4. 8T SRAM Cell Design Using FinFET**

FinFETs have emerged as the most suitable candidate for DGFET structure. Proper optimization of the FinFET devices is necessary for reducing leakage and improving stability in SRAM. The supply voltage (VDD), Fin height (Hfin) and Vth optimization can be used for reducing leakage in FinFET SRAMs by increasing Fin height which allows reduction in VDD. However, reduction in VDD has a strong negative impact on the cell stability under-parametric variations. We require a device optimization technique for FinFETs to reduce standby leakage and improve stability in an SRAM cell.

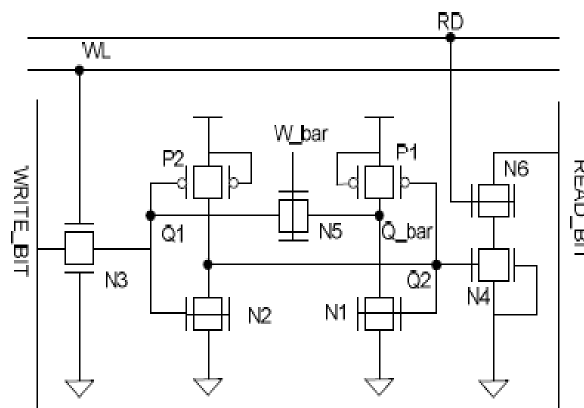


**Fig. 3 FinFET Based 8T SRAM Cell**

SRAM cells are used to implement memories that require short access times, low power dissipation and tolerance to environmental conditions. Earlier works [11-12] have shown that FinFET based 8T SRAM design shown improved performance compared to CMOS based design. Functionality and tolerance to process variation are the two important considerations for design of FinFET based 8T SRAM at 22nm technology. Proper functionality is guaranteed by designing the SRAM cell with adequate low leakage current and lower power consumption.

## 5. Results and Simulation

### A. Cell Delay

The time delay between 50% activation of read enable to when the sense amplifier output has reached 90% of its full swing is called as read delay [13]. Read operation is performed through p-type read access FinFET (P4) and read bitline (BLT). "The time delay between 50% activation of write enable to when node q is 90% of its full swing is called as write delay" [13]. Write operation is performed through n-type write access FinFET (N3) and write bitline (BLC). It is to be noted that the compliment of the data to be written is carried by BLC.

### B. Power Dissipation

Power dissipated by the circuit at operation condition. Here we will calculate active power at 22nm technology. The power dissipation includes both dynamic and static power. The static power involves power dissipation when the gate is not switching and the dynamic power involves the power dissipation during switching. So

$$P_{active} = P_{dynamic} + P_{static} \quad (1)$$

$$P_{active} = P_{switch} + P_{short} + P_{leak} \quad (2)$$

$$P = \alpha_{0\to1} \times C_1 \times F_{clock} \times V_{dd}^2 + I_{short-circuit} \times V_{dd} + I_{leakage} \times V_{dd} \quad (3)$$

Where $\alpha_{D-1}$ =Probability, $C_1$=Load capacitance, $F_c$=clock frequency, $V_{dd}$ =Power supply, $I_{short}$ =Short circuit current, $I_{leak}$= Leakage current.

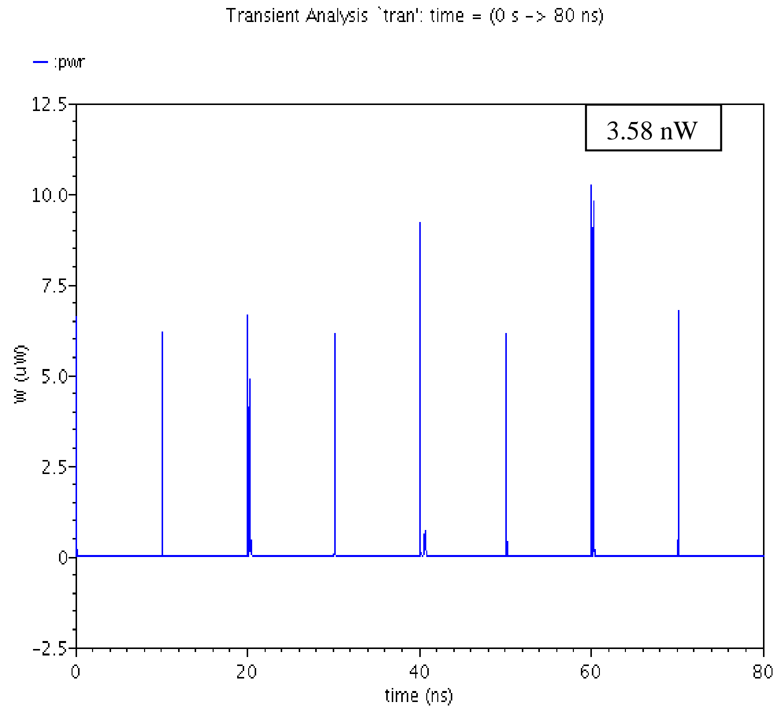


**Fig. 4 Power Dissipation of 8T SRAM cell**

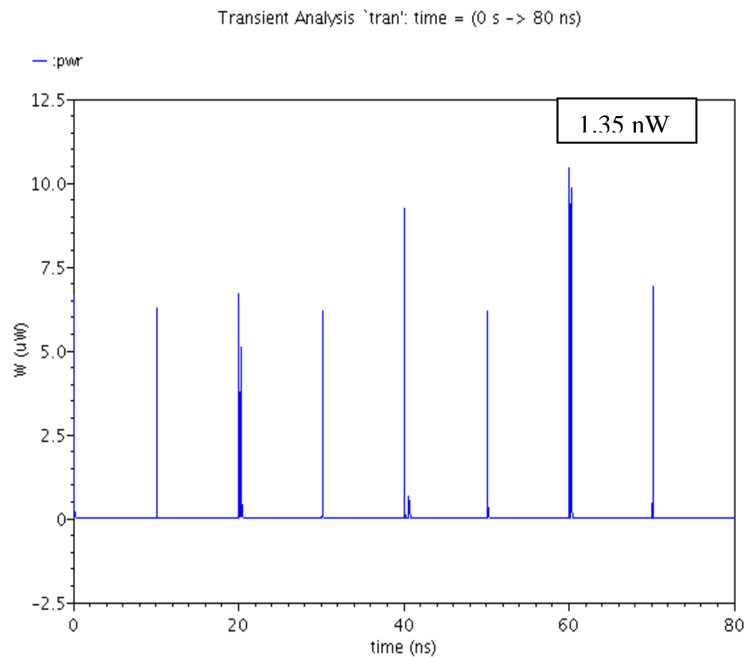


**Fig 5: Power Dissipation of FinFET 8T SRAM cell**

**Table 1 Power dissipation of 8T SRAM and 8T FinFET SRAM cell at different voltage**

| Parameters | 8T SRAM cell | FinFET 8T SRAM cell |
|---|---|---|
| Supply Voltage (V) | 0.3 V | 0.3 V |
| Power(nW) | 3.58 | 1.35 |

**C.**

**Leakage Current**

Leakage current determined when the circuit is in idle mode. We measure the leakage current using FinFET technology. The basic equation of leakage current is [16]

$$I_{leakage} = I_{sub} + I_{ox} \quad (4)$$

Where, $I_{sub}$=Sub threshold leakage current.

$I_{ox}$ = Gate oxide current.

$$I_{sub} = K_1 W e^{-Vth/nV_0} \left[1 - e^{-\frac{V}{V_0}}\right] \quad (5)$$

Where k1 and n is experimentally derived, W is gate width, Vθ is thermal voltage, n slope shape factor/ sub threshold swing coefficient, $V_{th}$ is threshold voltage.

$$I_{ox} = K_2 W [\frac{V}{T_{ox}}]^2 e^{-\alpha T_{ox} /V_0} \quad (6)$$

Where $K_2$ and α are experimentally derived, Tox is oxide thickness

.**Table 2: Leakage current at various voltages.**

| Parameter | This Work | |
|---|---|---|
| | CN8T SRAM | 8T FinFET SRAM |
| Technology | 22 nm FinFET | |
| Supply Voltage (V) | 0.3 | 0.3 |
| Leakage Current (nA) | 4.35 | 2.83 |

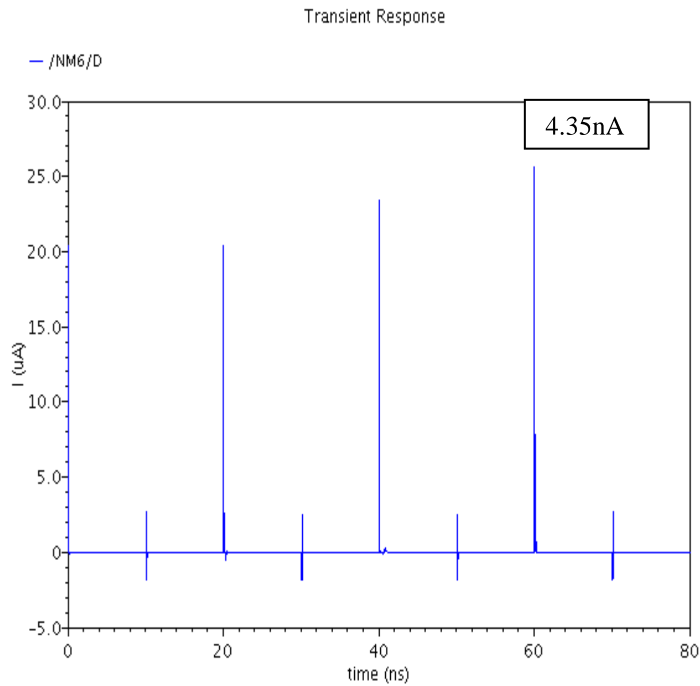


**Fig 6 leakage current of 8T SRAM cell**

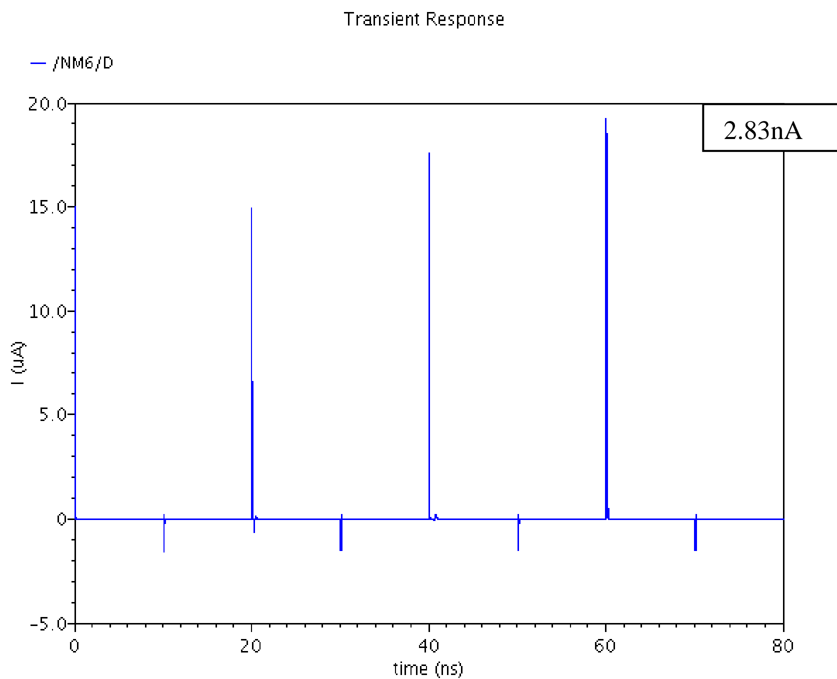


**Fig. 7 Leakage current of FinFET 8T SRAM cell**

**D. Leakage Power**

Stand by leakage power is measured at the time of idle mode. The equation of leakage power is

$$P_{leakage} = I_{leakage} \times V_{dd} \quad (7)$$

Where $P_{leak}$=Leakage power, $I_{leakage}$=Leakage current and $V_{dd}$ is supply voltage. According to the equation the power depends upon the leakage current and supply voltage.

**Table 3 Leakage power at various voltages.**

| Parameter | This Work | |
|---|---|---|
| | **CN8T SRAM** | **8T FinFET SRAM** |
| **Technology** | 22 nm FinFET | |
| **Supply Voltage (V)** | 0.3 | 0.3 |
| **Leakage Power (nW)** | 16.60 | 11.35 |

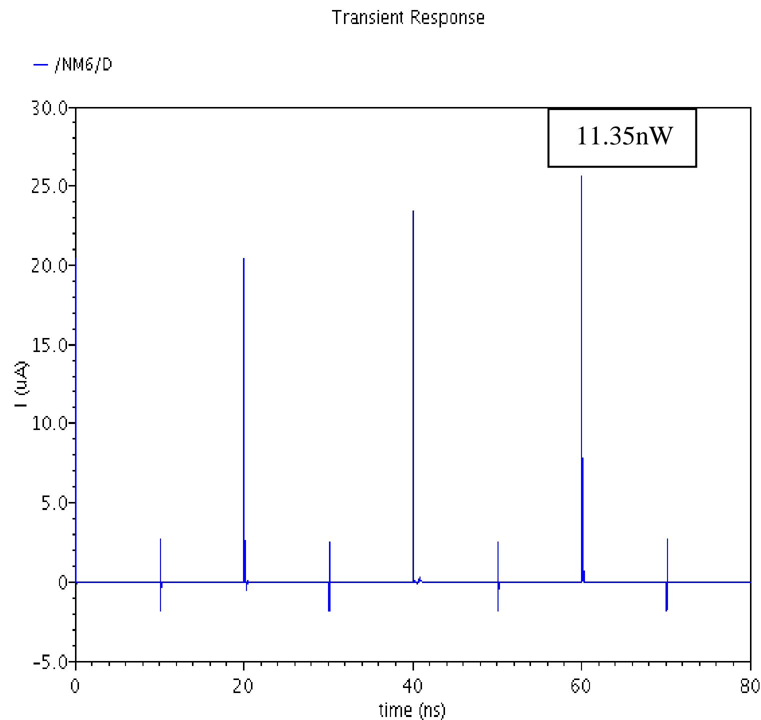


**Fig. 8 Leakage power of FinFET 8T SRAM cell**

### E. Read Stability and Write Ability

Static Noise Margin (SNM) is a major performance metric for analyzing SRAM cell stability [14]. It is the maximum noise which can be tolerated by the device. Stability of SRAM during read and write operations are called as Read Static Noise Margin (RSNM) and Write SNM (WSNM) respectively [14]. Read stability is determined by RSNM of the cell. Higher RSNM indicates good read stability while lower RSNM indicates poor read stability. Write ability of

SRAM cell is determined by WSNM. The width of the smallest square that can be embedded between the lower-right half of the curves is called as WSNM [15].

**Table 4 Comparison of RSNM and WSNM result**

| Parameter | CN8T SRAM | 8T FinFET SRAM |
|---|---|---|
| **Technology** | 22 nm FinFET | |
| **Supply Voltage (V)** | 0.3 | 0.3 |
| **RSNM (mV)** | 260.81 | 516.70 |
| **WSNM (mV)** | 272.50 | 530.30 |

## 6. Conclusion

Analysis of various parameters such as output, power dissipation, leakage current and leakage power of FinFET based 8T SRAM cell has been described in this paper. A FinFET 8T SRAM memory cell is proposed with improved leakage current and leakage power. To improve the read ability, an additional conducting p-type FinFET and a p-type FinFET read access transistor are used. The FinFET based 8T SRAM cell provides better results for improve the leakage current, leakage power WSNM and RSNM as compare to FinFET based 6T and 7T SRAM cells.

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